CMOS 5 VOLT/ 3 VOLT ANALOG SWITCH APPLICATIONS

INTRODUCTION

The ALD42XX CMOS analog switch family is designed for low voltage micropower systems where high precision and fast signal transfer are desired. The CMOS analog switches have essentially zero DC power consumption and are ideal for 5V or 3V battery operated portable systems which use mixed analog/digital signals. They are also compatible with microprocessor-based hand held systems, terminals and instruments.

These high speed precision rail-to-rail analog switches interface to standard CMOS input logic levels. They also provide excellent performance when used with the broad selection of single, dual and quad CMOS rail to rail operational amplifiers and other low voltage micropower linear components offered by Advanced Linear Devices.

GENERAL DESCRIPTION

The ALD4201/ALD4202M are quad CMOS analog switches specifically developed for 3 to 12 volt single power supply or ±1.5V to ±6.0V dual power supply applications where low voltage, low charge injection, and low leakage currents are important analog switch operating characteristics. Precision matching, charge compensation circuitry, fast switching, low transient current spikes, low on-resistance and micropower consumption are further benefits from this analog switch technology optimized for low voltage. The ALD4201 is designed to operate in break-before-make mode, where two analog channels sharing a common source are prevented from shorting together. The ALD4202M is designed to operate in make-before-break mode, intended for applications where continuous connection to a common source is imperative, as in an operational amplifier gain circuit where a closed loop circuit connection needs to be preserved at all times during signal and/or feedback resistor switching.

The ALD4201/ALD4202M are designed for precision applications such as charge amplifiers, sample and hold amplifiers, data converter switches, and programmable gain amplifiers. These switches are also excellent for general purpose switching applications for any low voltage and/or battery operated systems.

The ALD4211/ALD4212/ALD4213 quad CMOS analog switches are designed for ultra low charge injection applications using a single 3V to 12V power source. In the high precision mode, the input signals are connected to COM input pins and the analog switch outputs are the OUT pins, respectively. In this connection configuration, a very low charge injection of 0.2pC is achieved when sampling capacitors of 200pF are used.

In the general purpose application mode, the COM and the OUT terminals can be reversed, if necessary. The input signals, in this case, are connected to either the COM or the OUT terminals. The outputs of the analog switches are then the OUT or the COM terminals, corresponding to the other terminal of the analog switches.

SPECIAL DESIGN FEATURES

The ALD4201/ALD4202M quad SPST CMOS analog switches are ideal for applications using single power supplies ranging from 3V to 10V or dual power supplies from ±1.5V to ±5.0V. These analog switches feature industry standard pin configuration allowing simple PC board layout.

Especially designed for low charge injection, the ALD4211/ALD4212/ALD4213 CMOS analog switches can be used to improve switching transient signals in circuits that require a 1000pF or less sampling capacitor. These analog switches are also designed to operate with a 200pF sampling capacitor to provide five times faster effective signal capturing than with a 1000pF sampling capacitor.

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The ALD4211/ALD4212/ALD4213 feature very high precision due to these factors:

1. The analog switch has ultra low capacitive charge coupling so that the charge stored on a 200pF sampling capacitor is minimally affected.

2. With special charge balancing and charge cancellation circuitry designed on chip, the ALD4211/ALD4212/ALD4213 achieves ultra low charge injection of typically only 0.2pC resulting in extremely low signal distortion to the external circuit.

3. The analog switch switching transistors have pA leakage currents minimizing the droop rate of the sampling circuit.

4. The internal switch timing allows for the analog switch to turn off internally without producing any residual transistor channel charge injection, which may affect external circuits. With a low loss polystyrene or polypropylene sampling capacitor, long data retention times are possible without significant signal loss.

The ALD4211/ALD4212/ALD4213 CMOS analog switches, when used with industry standard pinout connection, have the input and output pins reversed with the signal source input connected to OUT pins and COM pins used as output pins. In this connection and when used with 1,000pF or greater value capacitors, or when connected to a DC current or resistive load, the switch would not be operating in an ultra low charge injection mode. Typical charge injection, in this case, would be 5pC as the pin to pin capacitive coupling effect would dominate. In this connection, all the other characteristics of the ALD4211/ALD4212/ALD4213 CMOS analog switches remain the same.

The ALD family of analog switches were developed with an ON-resistance matching of two percent between the different analog switches. The Total Harmonic Distortion of the analog signal through the switch is also minimized for the audio frequency range.

Chart 1 shows the salient characteristics of each of the switches in the ALD analog switch family. The ALD analog switch family is manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate process. They are designed to be used as linear elements in Advanced Linear Devices' Function-Specific ASIC.

DESIGN PRECAUTIONS

Connect all inputs of the unused switches to V+ or V-. The impedance of the inputs of the ALD 42XX CMOS analog switches is so high that the internal logic levels become undefined if the inputs are left disconnected. When left disconnected, both the internal P-channel and N-channel transistors may be in an unintended state where oscillation and intermittent excessive current drain may occur.

When connecting the analog switches to external circuits, care must be taken to insure that inductive or capacitive transient coupling does not cause malfunction or permanent damage to the analog switches. This is particularly important if the connections are made through long wires or signal lines.

To prevent latch up, it is necessary that the input and output voltage signals do not exceed the power supply rails by more than 0.3 volts. For example, when using a single 5 volt power supply, the input and output signals should never be more positive than 5.3 volts or more negative that -0.3 volts. When using dual $\pm$1.5 volt power supplies, the input and output signals should never be more positive than 1.8 volts or more negative than -1.8 volts.

SWITCHING LOW LEVEL SIGNALS

When switching low level signals, careful choice of a switch and design of the system layout helps avoid signal masking by AC noise pickup and DC voltages generated by thermocouple effects. Several factors must be considered for effective signal switching and transmission. For a system that has a significant signal path length and is potentially being routed in a noisy signal environment common mode signals may be picked up. This common mode signal can provide a significant error for low level signal transmission. To minimize the effect of common mode signals, use twisted pair of wires. The transmission cable carrying the transducer should be as short as possible to minimize noise. Signal conductors should be tightly twisted for minimum enclosed area. This technique guards against picking up electromagnetic interference and shields the twisted wire against capacitively coupled electrostatic interface charge. The transmission cable must present a balanced line to the source of noise interference. It must have an equal series impedance in each conductor and an equal series impedance to ground. The result should be that noise will be coupled in phase to both conductors and rejected as common mode voltages.

Silicon in contact with aluminum creates a thermocouple voltage. In a typical switch, the source voltage will be exactly cancelled by the drain voltage, but large thermal gradients between the source and drain contacts can produce a net offset voltage. The essentially zero current consumption of the ALD switch family translates into minimal errors due to thermocouple offsets.

	ALD4201	ALD4202M	ALD4211	ALD4212	ALD4213
Single Supply, 3 V - 10V	Yes	Yes	Yes	Yes	Yes
Dual Supplies ±1.5V to ±5V	Yes	Yes	Yes*	Yes*	Yes*
Power Dissipation, μW	0.1	0.1	0.1	0.1	0.1
Charge Injection, pC	1.0	1.0	0.2	0.2	0.2
Break-Before-Make	Yes	-	Yes	Yes	Yes
Make-Before-Break	-	Yes	-	-	-
Sampling Capacitor, pF	1000	1000	200	200	200
Rail to Rail Signal Levels	Yes	Yes	Yes	Yes	Yes
Rail to Rail Output Levels	Yes	Yes	Yes	Yes	Yes

INPUT LOGIC	SWITCH STATE			
	ALD4201	ALD4202M	ALD4211	ALD4212
0	ON	OFF	ON	OFF
1	OFF	ON	OFF	ON

INPUT LOGIC	SWITCH STATE			
	ALD4213			
	SWITCH 1	SWITCH 2	SWITCH 3	SWITCH 4
0	OFF	ON	ON	OFF
1	ON	OFF	OFF	ON

Chart 1

* Note : For dual supply operation, break-before-make timings are not guaranteed.

APPLICATIONS

The following examples are some of the applications and typical protection circuits of the ALD42XX CMOS analog switch family.

PROCESS CONTROL

A Process Control system may use transducers which convert physical variables such as pressure, temperature, acceleration, and flow to analog electrical signals. These analog electrical signals may be switched in sequence to a control system to perform specific functions as a result of these changing physical parameters.

If the same transducer is used in a number of locations the signal conditioning circuitry may be switched between sensors prior to amplification. A primary source of error with a low level signal may be the switching transients present in the switch. These transients are the result of charge injection from the switches, producing an error voltage which appears at the switch output. The lower the signal level, the greater the error introduced by the charge injection of the switch. The ALD switch family is ideally suited for this application. For example, the ALD4211/ALD4212/ALD4213, with an extremely low charge injection of 0.2pA, will create only microvolt offset errors when switching into a 200pF load. This is ideal for low level switching applications.

Differential signals can be generated by bridge-type transducers. These devices will produce a signal of two components, a difference signal superimposed on a common mode signal. The difference component subtracted from the common mode signal conveys the information. In this case two switches may be used, one in each leg of the bridge output. The voltage difference across the switches is the differential bridge output. This application is used for the rejection of unwanted common mode signal where elimination of electrical noise is a concern.

High level signals may be operated from rail to rail of the power supply. However, rail to rail power supply voltages must not be exceeded as damage may occur to the device.

Figure 1
Input Noise Filter Circuit

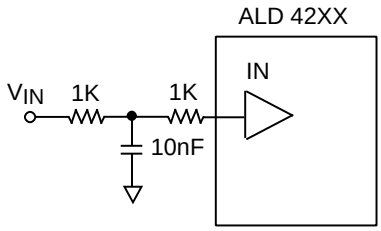


Figure 2
Input Surge Protection

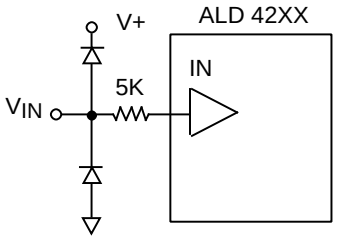


FIgure 3
Signal Source Surge Protection

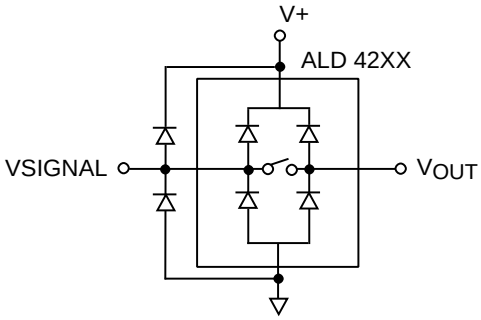
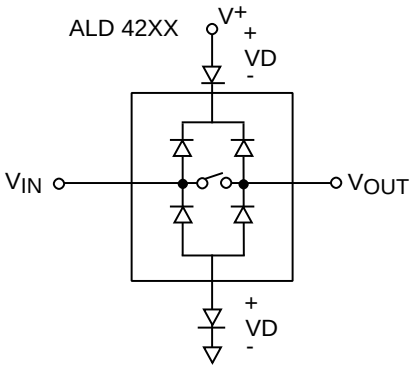


FIgure 4
Overvoltage Surge Protection



$V_{OUT_{MAX}} = V_{IN_{MAX}} = V^+ - V_D$
$V_{OUT_{MAX}} = V_{IN_{MAX}} = V_D$

Figures 1, 2, 3, and 4. Excessive Internal Noise Suppression Circuits.

Figure 1 illustrates an example of an input signal from a network where excessive external noise can be filtered out before it is applied to the switch input. If the interface circuits are from a system with different power sources or with uncontrolled power-on sequences, various input signal surge protection circuits such as shown in **Figures 2, 3 and 4** may be required.

For any given application, the user must take into consideration the different power supplies, the power-on sequences in the different parts of the system, and the extent of any overvoltage condition when deciding on the appropriate surge protection circuitry.

Figure 5
Oscillation Circuit

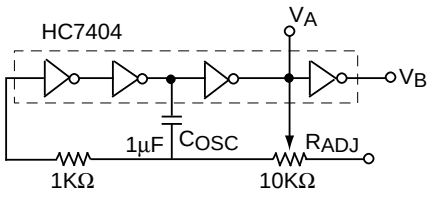
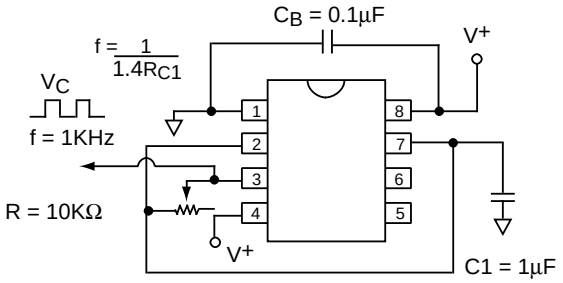


Figure 6
ALD 555 Oscillation Circuit



Figures 5 and 6. Basic Building Blocks are the basic oscillator circuits used as building blocks in many of the application circuits below.

Figure 5 uses gates of the HC7404 with passive components to provide complementary non-overlapping clock outputs. The clock outputs are Va and Vb where Vb is complementary to Va.

Figure 6 uses the ALD555 timer to provide a simple single output oscillator. The clock output is Vc.

Figure 7
Selectable Gain Amplifier With
Make-Before-Break Switching

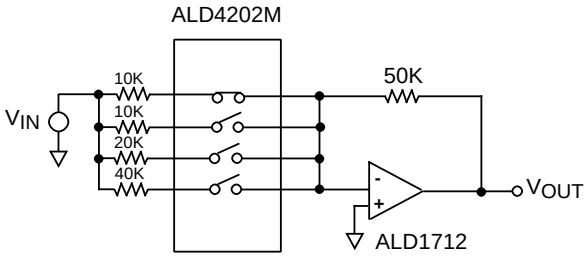
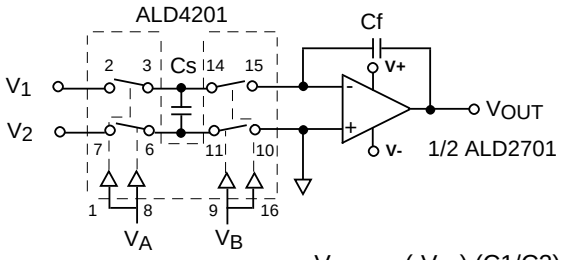


Figure 7. Programmable Amplifier Gain with Make-Before-Break Switching. The ALD4202M make-before-break switch is especially useful in selectable gain amplifier circuits to minimize switching noise. Each input is switched selectively with the previous switch remaining closed until the new switch is closed. The amplifier gain is a function of the resistor ratios. Different resistors may be switched in to change the gain of the amplifier.

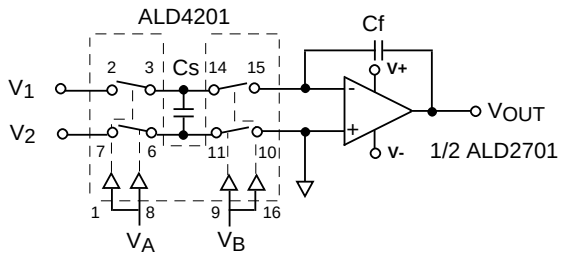
Figure 8
Precision Voltage Inverter



$V_{OUT} = (-V_{IN})\ (C1/C2)$
$C1 = C2 = 1\mu F$
$ERROR \approx 0.2\%$

Figure 8. Precision Voltage Inverter. A precision voltage inverter can be built using one ALD4201 and a simple oscillator circuit. The oscillator in figure 5 provides outputs Va and Vb where Vb is the complement of Va. The oscillator output signal and its complement are connected to the inputs of the ALD4201 switches. When the two switches to the left of C1 are closed, and the two to the right of C1 are open, C1 is charged to Vin. Then the two switches to the left of C1 open and the switches to the right of C1 close causing the transfer of charge from C1 to C2. After a number of cycles C2 is charged to the input voltage. As C2 is isolated from the input, grounding the positive side of C2 will cause the output voltage (V_{OUT}) to be the negative of V_{IN}. This circuit can achieve an error as low as 0.2% because of the low charge injection and low leakage current in the switches.

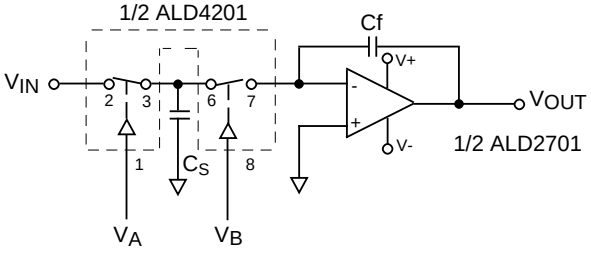
Figure 9
Differential Integrator With
Frequency Controlled Gain



$V_{OUT} = -fs\ (Cs/Cf) \int (V_1 - V_2)\ dt$
For Cf = Cs = 1000pF, $V_{OUT} = (-fs)\ (V_{IN}\ \Delta t)$

Figure 9. Differential Integrator With Frequency Controlled Gain. The ALD4201 analog switches are used to transfer the differential voltage (V_1-V_2) to the inputs of the operational amplifier. The switches to the left of C_S close and the switches to the right open causing capacitor C_S to be charged to the input voltage (V_1-V_2). Then the switches to the left of C_S open and the switches to the right close. The voltage is then integrated to produce the output. The oscillator circuit of figure 5 is used. The gain of the integrator can be easily controlled by varying the oscillator frequency.

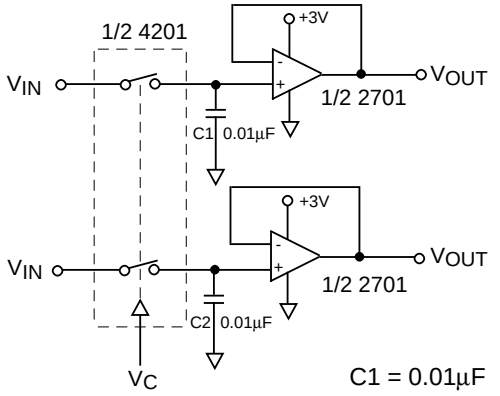
Figure 10
Inverting Switched Capacitor Integrator



$V_{OUT} = -fs\ (Cs/Cf) \int (V_{IN})\ dt$
For Cf = Cs = 1000pF, $V_{OUT} = (-fs)\ (V_{IN}\ \Delta t)$

Figure 10. The Inverting Switched-Capacitor Integrator. This is another integrator circuit similar to Figure 9 except only half of an ALD4201 is used due to the single input. The oscillator in figure 5 is used.

Figure 11
Switched-Capacitor Frequency Controlled
Gain Amplifier



$V_{IN} \geq 10mV$ VOUT ERROR < ±2%

fs = (1KHz) (f in) = 1KHz to 50KHz

$$V_{OUT} = \frac{(F\ in)}{(fs)} \frac{(C1\ V_{IN})}{(C2)}$$

For f in = fs, $V_{OUT} = 10\ V_{IN}$

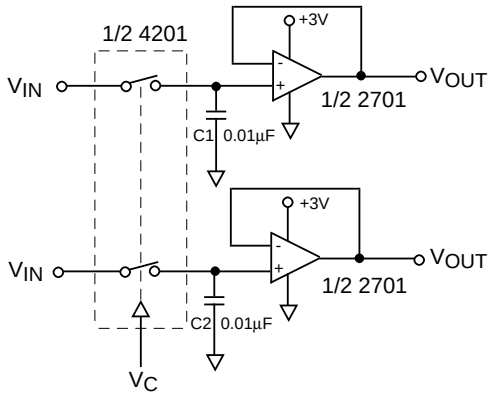
Figure 11. The Switched Capacitor Frequency Controlled Gain Amplifier. This circuit is very common in variable gain amplifier circuits because the gain of the amplifier can be easily controlled by changing the sampling frequency. Figure 11 uses two ALD4201, three capacitors, an ALD1712 operational amplifier, two inverters and a 1KHz oscillator (Figure 6) to form the variable gain amplifier.

The operation of the circuit in Figure 11 is as follows: First consider capacitor C1. At *t* 1 (two switches to its left close and the two to its right open), C1 is charged to V_{IN}. The charge stored in C1 is Qc1=(V_{IN})(C1). At *t* 2 (two switches to the left of C1 open and two switches to the right of C1 close). C1 discharges to zero volts. Current *i* 1= dQ (C1)/ dt = (*f* in)(C1) (V_{IN}), (dt = 1 / *f* in). Next consider capacitor C2. At *t* 3 (two switches to its left close and the two to its right open), C2 is discharged to zero volts. At *t* 4 (two switches to the left of C2 open and the two to its right close), C2 is placed in parallel with C3 and is charged up to Vout with the stored charge Q = (V_{OUT})(C2). Thus, current *i* 2 can be represented as *i* 2 = dQ/dt = fs (V_{OUT}) (C2).

i 1 = *i* 2, *i* 1 - *i* 2 = 0
f in C1 V_{IN} = *f* s C2 V_{OUT}
Vout = (*f* in)(C1) (V_{IN})/ *f* s C2
For C1 = 0.01µF, C2 = 0.001µF
and *f* s = *f* in, $V_{OUT} = 10\ V_{IN}$

The gain of the amplifier is controlled by the ratio of oscillators *f* in and *f* s. The frequency *f* s is normally fixed at 1KHz. The gain of the amplifier is then set by the frequency *f* in where Gain = V_{OUT}/V_{IN} = 10N (N is the ratio of *f* in to *f* s). For example, varying the input frequency *f* in from 1KHz to 50KHz will change the amplifier gain linearly from 10 to 500. This circuit is particularly useful in computer programmed circuits where the gain can be digitally controlled by varying the input oscillator frequency as a sub-frequency of the master clock.

Figure 12
Low Voltage Sample and Hold Circuit



See Figure 6

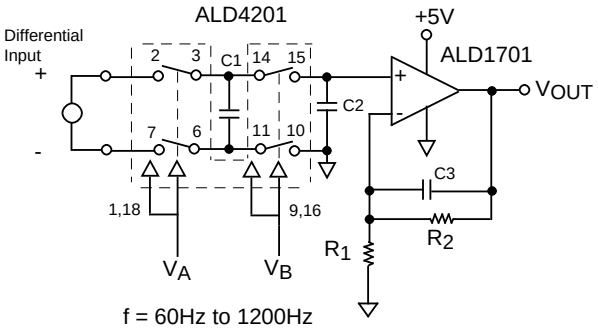
f = 2Hz to 200KHz
Droop rate = 1 mV/sec

Figure 12. Low Voltage Sample and Hold Circuit. Sample and hold circuits are widely used in analog signal processing and data conversion systems to store analog voltages accurately over time periods. Applications include data distribution systems, digital volt meters, signal reconstruction filters, and analog computational circuits.

A simple low voltage sample and hold circuit is constructed by using half of an ALD4201 analog switch and half of an ALD2701 operational amplifier. During the sample phase the switch is closed and the hold capacitor is charged to the input voltage. Once the capacitor is charged to its final value, the hold mode is entered by opening the switch. During the hold mode the capacitor voltage can be examined by the low leakage buffer.

Because of the low charge injection and low leakage current in the switches, this circuit can obtain very precise outputs with a droop rate of only 1mV/sec. This type of circuit finds a wide range of applications in battery operated portable systems because of its low operating voltage range.

Figure 13
Differential Input to Single Ended Output Converter With Gain



f = 60Hz to 1200Hz

V_{OUT} = 1+ R2/R1 = 101V_{IN}
C1 = C2 = C3 = 1µF R1 =1KΩ, R2 = 100KΩ
V_{OUT} = 5V Full Scale
Error = 1%

Figure 13. Differential Input to Single Ended Output Converter With Gain. This is used to convert a differential input signal to a single input signal and uses oscillator, as shown in Figure 5. The differential input signal, Vin, is converted to a single input signal at the positive input of the operational amplifier through one ALD4201 and two capacitors. The charge transferring technique in this circuit is similar to the previous circuits shown in Figures 8 and 9. The amplifier, ALD1701, provides a fixed gain of (1+R2/R1).

Figure 14
Multiply By 2 Circuit

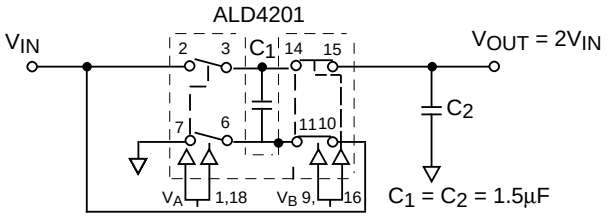


Figure 15
Divide By 2 Circuit

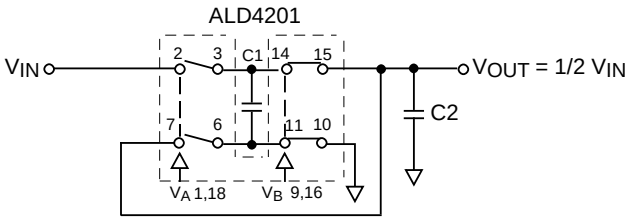


Figure 14. Multiply-By-2 Circuit is constructed by using one ALD4201 and capacitors C1 and C2 (See oscillator in figure 5 for switch driver). When the two switches to the left of C1 are closed, and the two to its right are open, C1 is charged to V_{IN}. When the two switches to left of C1 are open and the two to its right are closed, the negative side of C1 (previously at ground) is now connected to V_{IN}. However, the voltage across C1 cannot change instantly. As a result, the voltage at the output V_{OUT} becomes twice V_{IN} . C2 is used to store the voltage at V_{OUT} when the switches return to the original positions.

Figure 15. Divide By 2 Circuit. When switches to the right of C1 are open and switches to the left of C1 are closed, C1 is in series with C2. As C1 and C2 are of equal value the voltage across C1 equals the voltage across C2 equals 1/2 V_{IN}. When switches to the right of C1 are closed and switches to the left of C1 are open C1 is in parallel with C2 maintaining the charge across C2. The oscillator in Figure 5 is used to drive the switches.

Figure 16. Digitally Controlled Precision Multiply or Divide By 2 Circuit combines the functions of the Multiply-By-Two circuit of Figure 14 with the Divide-By-Two circuit of Figure 15. The circuit is constructed by using two ALD4201 QUAD switches and two matched capacitors C1 and C2 (locate oscillator in Figure 5 for switch driver). In each case two switches are driven in parallel. A,B,C,D are the switch drivers which are controlled by a single digital input and an inverter.

To operate the "multiply by two circuit", a "0" digital input opens switches B & C and closes switches A & D. For the "divide by two circuit", a "1" digital input closes switches B & C and opens switches A & D.

Figure 16
Digitally Controlled Precision
Multiply Or Divide By 2 Circuit